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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/650,719	05/20/1996	JEFFREY S. MAILLOUX	303.623US1	2941

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EXAMINER	
KIM, HONG CHONG	

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08650719	5/20/96	MAILLOUX ET AL.	303.623US1

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 08/650,719
Filing Date: May 20, 1996
Appellant(s): MAILLOUX ET AL.

Mark V. Muller
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/8/2007 and 8/13/2007 appealing from the Office action mailed 2/20/2007 and 7/12/2007 respectively.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

A Statement identifying related appeals and interferences in the brief is correct (see below).

"A first, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,561 (Atty. Ref. No. 303.623US6). However, a Notice of Allowance indicating allowance of all claims was subsequently marled to the Appellant, and the application has now issued as U.S. Pat. No. 6,615,325. This matter never appeared before the Board.

A second, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,560 (Atty. Ref. No. 303.623US2). The Board issued a decision in this matter, allowing all claims (Appeal 2004-0414, attached hereto), and the application has now issued as U.S. Pat. No. 7,103,742. This matter is no longer before the Board.

A third, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,701 (Atty. Ref. No. 303.623US5). The Board issued a decision in this matter, allowing all claims (Appeal 2004-1705, attached hereto). The application has not yet issued, and is no longer before the Board.

A fourth, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,562 (Atty. Ref. No. 303.623US3). The Board issued a decision in this matter, allowing all claims except claim number 61 (Appeal 2005-1725, attached hereto), and the application has now issued as U.S. Pat. No. 7,124,256. This matter is no longer before the Board.

A fifth, related appeal was filed with respect to U.S. Patent Application Serial Number 08/984,563 (Atty. Ref. No. 303.623US4). Since this fifth appeal was only recently filed (on January 25, 2007), the matter is still pending before the Board.

An appeal was filed with respect to the instant matter (U.S. Patent Application Serial Number 08/650,719; Atty. Ref. No. 303.623US1) on January 16, 2004. Prosecution was reopened by the Examiner, and a supplemental appeal brief was filed August 11, 2004. Prosecution was again reopened by the Examiner, and after receiving a final rejection, the Appellant has filed this Appeal in response."

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct. The appellant did not response the double patenting rejection on claims 59-60, therefore the appellant concedes that the double patenting rejection on claims 59-60 is proper.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5610864	Manning	3-1997
6065092	Roy	5-2000
5293347	Ogawa	3-1994

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following ground(s) of rejection are applicable to the appealed claims:

Claim 61 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in

the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Because although the specification (Figs. 9, 12 and page 30 line 24 thru page 33 line 21) describes burst and pipeline operations as pointed out by the applicants in the brief, the specification does not specifically describe claimed limitation of "providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipelined mode of operation", "switching mode to a burst mode of operation", "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation", and "providing a new external addresses for every access associated with accessing the asynchronously-accessible memory device while in the burst mode of operation".

This instant application describes "switching between burst EDO and pipelined EDO modes is accomplished on successive /CAS cycles" (Pg 38 lines 11-15 and Fig. 17 Refs 114 and 115, each /CAS cycle represents a new column address in pipeline mode). In other words, a new external address (Fig. 17 3rd addr) is needed after the initial external address (Fig. 17 2nd addr) to switch modes (also refer to claim 46 of the present application), however, applicant claimed generating at least one subsequent internal address patterned without a new external address. Therefore, "providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipelined mode of operation", "switching mode to a burst mode of operation", "while in the burst mode of operation, generating at least one

subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation", and "providing a new external addresses for every access associated with accessing the asynchronously-accessible memory device while in the burst mode of operation" were not described in the specification. Again pg. 33, lines 13-21, pg 38, lines 11-15, and pg. 27, lines 5-11 of this instant application do not specifically disclose "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-9, 33-35, 46, 48-50, 59-60, and 63-64 are rejected under 35 U.S.C. 103(a) as obvious over by *Manning*, U.S. Patent 5,610,864 in view of Roy U.S. Patent No. 6,065,092 or *Ogawa* U.S. Patent 5,293,347.

As to claim 50, *Manning* discloses the invention as claimed. *Manning* discloses a system comprising: a microprocessor (Fig. 11 Ref. 112); a memory (Fig. 11 Ref. 124) coupled to the microprocessor, the memory selectively operable either in a burst mode (col. 6 lines 14-34 and col. 7 lines 43-54) or fast page mode, EDO page mode, static column mode, wherein the memory is an asynchronous dynamic random access memory (Fig. 1 and EDO constitutes asynchronous memory, col. col. 6 lines 14-16, since the EDO does not require a system clock to operate); and a system clock (col. 8 line 46) coupled to the microprocessor.

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically discuss the detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write

circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have been a highly desirable feature in the memory environment of Manning because one of the objectives of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle.

Alternatively, Ogawa discloses the memory operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 63, *Manning* discloses a storage device, comprising; an array of memory cells (col. 4 lines 13-15); mode circuitry for receiving a burst/page signal (col. 6 lines 14-26 and col. 7 lines 40-55); and operation circuitry operable in a burst or a EDO page mode of operation depending upon the burst/page signal, the operation circuitry switchable between burst and page modes of operation (col. 5 lines 41-50, col. 6 lines 14-34, and col. 7 lines 40-55).

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically discuss the detailed operation of a pipeline signal/mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline signal/mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write

circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline signal/mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline signal/mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have been a highly desirable feature in the memory environment of Manning because one of the objectives of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page signal/mode of Manning to a pipeline signal/mode of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle.

Alternatively, Ogawa discloses the memory operable in a pipeline signal/mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline signal/mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page signal/mode of Manning to a pipeline signal/mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 1, *Manning* discloses the invention as claimed. *Manning* discloses an asynchronously accessible storage device (Fig. 1 and EDO constitutes asynchronous memory, col. col. 6 lines 14-16, since the EDO does not require a system clock to operate) comprising mode circuitry to select between a burst mode (col. 6 lines 14-34 and col. 7 lines 43-54) and a EDO page mode (col. 6 lines 14-21 and col. 7 lines 40-55); and circuitry operable in either the burst mode or the page mode coupled to the mode

selection circuitry and configure to select between two modes.(Fig. 1 Ref. 40 and col. 6 lines 14-21, col. 5 lines 41-50, and col. 7 lines 40-55).

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically discuss the detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read

and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have been a highly desirable feature in the memory environment of Manning because one of the objectives of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline

mode of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle.

Alternatively, Ogawa discloses the memory operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 2, Manning further discloses the burst mode and the pipelined mode are EDO modes of operation (col. 5 lines 41-50, col. 6 lines 14-34 and col. 7 lines 43-54)

As to claim 3, Manning further discloses the pipelined mode is an EDO mode (col. 5 lines 41-50, col. 6 lines 14-34 and col. 7 lines 43-54).

As to claim 4, Manning further discloses the burst mode is and EDO mode (col. 6 line 15).

As to claim 5, Manning further discloses the mode circuitry includes a buffer, the buffer for storing an address (Fig. 1 Refs. 18, 22, and 30).

As to claim 6, Manning further discloses the mode circuitry includes at least one counter for incrementing the address (Fig. 1 Ref. 26 and col.5 lines 51-62).

As to claim 7, Manning further discloses the mode circuitry includes receiving an external address (Fig. 1 Ref. 16 and col. 4 lines 16-28).

As to claim 8, Manning further discloses the mode circuitry includes a buffer, the buffer for storing an address (Fig. 1 Refs. 18, 22, and 30).

As to claim 9, Manning further discloses the mode circuitry includes multiplexed device for providing an internally generated address to the storage device (Fig. 1 Refs.

26 and 30 and col. 5 lines 51-62 & col. 3 lines 20-23, selection of external or internal address reads on this limitation).

As to claims 33, 59, and 60, *Manning* discloses a method for accessing a storage device (Fig. 1), comprising: receiving a first address to the storage device (Fig. 2 ROW); selecting between an asynchronously accessible (Fig. 1 and EDO constitutes asynchronous operation, col. col. 6 lines 14-16) burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and a EDO page mode (col. 6 lines 14-21 and col. 7 lines 40-55); selecting between outputting information from the storage device and inputting to the storage device (Fig. 2 /WE, read and write operations read on this limitation); obtaining a second address to the storage device (Fig. 2 /COL), and asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second addresses (Fig. 2, DQ and col. 5 lines 41-50, col. 6 lines 14-26 & col. 7 lines 43-54).

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be

used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically discuss the detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have been a highly desirable feature in the memory environment of Manning because one of the objectives of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle.

Alternatively, Ogawa discloses the memory operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput

or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 34, Manning further discloses a step of switching between the pipelined mode and burst mode (col. 5 lines 41-50, col. 6 lines 14-16 and col. 5 lines 42-50).

Roy also further discloses a step of switching between the pipelined mode and burst mode (col. 27 lines 35 thru col. 28 lines 48 and col. 21 lines 61-62 specifically col. 27 lines 54-58)

As to claim 35, Manning further discloses the second address is an external address (Fig. 1 Refs 16 and 30 and col. 4 lines 16-28 & col. 5 lines 42-55). Roy also further discloses the second address is an external address (col. 28 lines 16-25).

As to claim 46, *Manning* discloses a method for accessing several different locations in an asynchronously a storage device (Fig. 1 and EDO constitutes

asynchronous operation, col. col. 6 lines 14-16), comprising: selecting a EDO page mode (col. 6 lines 14-21 and col. 7 lines 40-55); providing a new external address with asynchronously-accessible memory device in the page mode of operation (col. 6 lines 14-21 and col. 7 lines 40-55); switching modes to a burst mode of operation (col. 6 lines 14-21 and col. 7 lines 40-55); providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67); and generating at least one subsequent internal address patterned after the initial external address while in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67).

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically discuss the detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read,

memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline mode and providing a new external address for every access associated with asynchronously-accessible memory device in the pipeline mode of operation (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed.

The ability to provide a new column address every cycle would have been a highly desirable feature in the memory environment of Manning because one of the objectives of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode and providing a new external address for every access associated with asynchronously-accessible memory device in the pipeline mode of operation of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle.

Alternatively, Ogawa discloses the memory operable in a pipeline mode and providing a new external address for every access associated with asynchronously-accessible memory device in the pipeline mode of operation (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput

or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode and providing a new external address for every access associated with asynchronously-accessible memory device in the pipeline mode of operation of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claims 48 and 49, Roy further discloses column, row, application, fixed access based switching (col. 27 lines 54-58) for the burst mode and the pipelined mode.

As to claim 64, *Manning* discloses a memory circuit, comprising; an array of memory cells (col. 4 lines 13-15); burst/page selection circuitry for determining a burst or a page mode of operation of the memory circuit (col. 5 lines 41-50, col. 6 lines 14-34 & col. 7 lines 40-55); and mode circuitry capable of operation in either a burst mode or a EDO page mode of operation, and switchable between burst and page modes of operation (col. 5 lines 41-50, col. 6 lines 14-34 & col. 7 lines 40-55).

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete.

In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically discuss the detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have been a highly desirable feature in the memory environment of Manning because one of the objectives of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle.

Alternatively, Ogawa discloses the memory operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

(10) Response to Argument

Response to argument regarding the rejection of claims 1-9, 33-35, 46, 48-50, 59-60 and 63-64 under 35 U.S.C. 103(a).

A. Appellants' argument on pages 13-16 in the Appeal Brief on 8/13/07 that "the combination of references does not teach all limitations" has been fully considered but it is not persuasive.

First of all, in response to appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which appellant relies (i.e., "true pipelined and burst operation "on the fly"" and "row-based

switching operation") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Manning discloses a memory selectively operable either in a burst mode (col. 6 lines 14-34 and col. 7 lines 40-55) or fast page mode, EDO page mode, static column mode (col. 6 lines 14-21 and col. 7 lines 40-55).

Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55). In other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically discuss the detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the

purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed.

The ability to provide a new column address every cycle would have been a highly desirable feature in the memory environment of Manning because one of the objectives of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient

suggestion and motivation to one of ordinary skill in the memory art to include the memory operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle and because the modification or substitution of well known one mode, fast page mode, EDO page mode, static column mode and burst operation for the other mode, a pipeline mode, to achieve the predictable result of the pipeline operation.

Alternatively, Ogawa discloses the memory operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline

mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Therefore, the combination of references discloses all limitations.

B. Appellants' argument on pages 16-17 in the Appeal Brief that there is "No motivation to combine the references" and "No reasonable expectation of success" has been fully considered but it is not persuasive.

In response to appellant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, *Manning* discloses a memory selectively operable either in a burst mode (col. 6 lines 14-34 and col. 7 lines 40-55) or fast page mode, EDO page mode, static column mode (col. 6 lines 14-21 and col. 7 lines 40-55).

Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per

cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55). In other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically discuss the detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed.

The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase the memory throughput or speed in Manning by providing a new column address every cycle and because the modification or substitution of well known one mode, fast page mode, EDO page mode, static column mode and burst operation for the other mode, a pipeline mode, to achieve the predictable result of the pipeline operation.

Alternatively, Ogawa discloses the memory operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Therefore, the references discloses motivation to combine the references and reasonable expectation of success.

(11) Related Proceeding(s) Appendix

Copies of the court or Board decision(s) identified in the Related Appeals and Interferences section of this examiner's answer are provided herein.

Copies of the decisions in related appeals are 2004-0414, 2004-1705, and 2005-1725.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Hong Kim

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